COMPUTER-AIDED DESIGN OF MICROWAVE PARAMETRIC FREQUENCY DIVIDERS

Alessandro LIPPARINI [1], Ernesto MARAZZI [2] and Vittorio RIZZOLI [1]

[1] Istituto di Elettronica - University of Bologna - Villa Griffone - 40044 Pontecchio Marconi - Bologna - ITALY
[2] SIAE Microelettronica S.p.A. - Via Buonarroti 21 - 20093 Cologno Monzese - Milano - ITALY

ABSTRACT

A straightforward computer approach to the design of parametric frequency dividers using microwave diodes is presented. A detailed characterization of the nonlinear element together with a new optimization philosophy make an accurate nonlinear design of MIC dividers directly affordable.

Introduction

Hybrid IC microwave frequency dividers still provide the only means of locking RF sources above 2 GHz to low-frequency reference oscillators by use of commercially available components. In particular, parametric dividers using microwave diodes often represent an optimum choice because of their broader bandwidth and much simpler circuit configuration as compared to the Miller or to the injection-locked types[1]. However, despite of the considerable technical interest of these devices, little information is available from the literature concerning the very basic problem of how to approach the design of a practical parametric divider in a systematic and cost-effective way. In particular, recent work on divider circuits using high-frequency (such as GaAs) varactors operated in forward-bias conditions [2] or even step-recovery diodes [3], seems to be mostly aimed at the presentation of empirical results, and still make reference to classic simplified analyses [4].

On the contrary, in this paper we outline an accurate and straightforward design approach based on a complete physical characterization of the microwave diode and on modern computer-aided methods for steady-state analysis of nonlinear networks [5,6].

Simulation of the active device

The key point for the validity of the computer-aided approach is an accurate model of the diode accounting for all main aspects of its RF performance. To obtain this, we write the current-voltage relationship in the form

$$i = I_S\left\{\exp\left(\frac{e\,v}{n\,K_B\,T}\right) - 1\right\} + \frac{d}{dt}\{q(v)\} \qquad (1)$$

where

i = diode current
v = voltage across the junction
q = total stored charge
I_S = saturation current
e = electron charge
K_B = Boltzmann's constant
T = absolute temperature
n = slope factor of current.

In general, there will be two main contributions to the stored charge, that is, the depletion-layer charge q_T and the charge due to injected minority carriers q_D. Thus

$$q(v) = q_T(v) + q_D(v) \qquad (2)$$

The first contribution is easily obtained from well-known expression for the depletion-layer differential capacitance, i.e.:

$$\frac{dq_T}{dv} = C_{TO}\left(1 - \frac{v}{\phi}\right)^{-\gamma} \qquad (3)$$

where ϕ is the diffusion potential and C_{TO} is the zero-bias transition capacitance. Thus

$$q_T(v) = \frac{C_{TO}\,\phi^{\gamma}}{\gamma - 1}\,(\phi - v)^{1-\gamma} \qquad (4)$$

valid for $v < \phi$ (forward voltages are taken as positive).
For $\gamma > 1$, (4) yields $q_T = 0$ as v approaches ϕ; in these cases we can assume

$$q_T(v) = 0 \qquad v \geq \phi \qquad (5)$$

since the depletion layer then vanishes. On the other hand, for hyperabrupt varactors with $\gamma > 1$, (4) fails for $v = \phi$; however, such diodes are usually strongly reverse-biased and it can be assumed that they are never operated in forward-bias conditions. Thus (4) and (5) can be used in general for computing the depletion-layer charge.
From p-n junction theory, the minority-carrier charge stored in the diode can be expressed as [7,8]

$$q_D(v) = n\frac{K_B\,T}{e}\,C_{DO}\,\exp\left(\frac{e\,v}{n\,K_B\,T}\right) \qquad (6)$$

($n = \frac{4}{3}$ in Moll's classic analysis [7]).
A simple expression for C_{DO}, which is sufficiently accurate for our present purposes, is obtained from [7]:

$$C_{DO} \simeq \frac{e}{n\,K_B\,T}\,I_S\,\tau \qquad (7)$$

where τ is the average minority-carrier lifetime (usually given by the manufacturer).
The current arising from (6) may represent an important contribution to the total diode current for a junction diode operated under forward-bias conditions. In these cases, the strong nonlinearity of (6) usually turns out in a significant improvement of power-handling ability, and possibly of circuit efficiency. Furthermore, through (1) and (6) the simulation of step-recovery diodes be-

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comes possible [9]. In such devices the storage capacitance dominates [7], i.e., on the average q_D is large compared to q_T, and the depletion-layer capacitance merely acts as a parasitic effect.

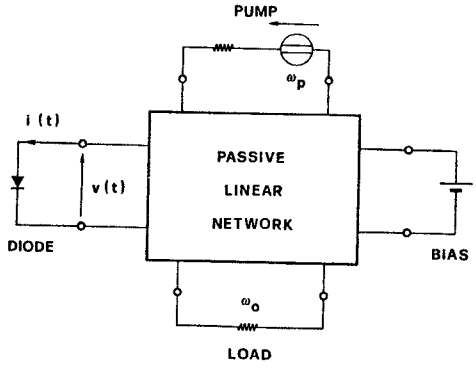

Fig. 1 Schematic representation of parametric frequency divider.

Design method

We consider the general circuit configuration of fig. 1, where the passive linear network includes idlers, filters, couplers etc., as well as the diode series resistance (assumed constant) and package parasitics. For a frequency divider by m with a fundamental output frequency ω_0, only one sinusoidal source (pump) at a frequency $\omega_p = m\,\omega_0$ will appear in the network.

Given a passive network, a steady-state *analysis* of the circuit may be carried out by the harmonic-balance technique [6]. According to this method, we represent both voltage and current at the diode terminals as periodic functions of time (having period $T_0 = \frac{2\pi}{\omega_0}$) of the form

$$v(t) = \mathrm{Re}\left\{ \sum_{k=0}^{N} V_k \exp\left(jk\omega_0 t \right) \right\}$$
$$i(t) = \mathrm{Re}\left\{ \sum_{k=0}^{N} I_k \exp\left(jk\omega_0 t \right) \right\}, \qquad (8)$$

where V_k, I_k are complex quantities and N is the total number of significant harmonics. Starting from a set of voltage harmonics V_k, we compute v(t) from the first of (8), then i(t) by means of the diode equation (1) and the Fast Fourier Transform algorithm, and finally the current harmonics I_k, again by use of the FFT. Now, according to the equations of the linear network, the voltage harmonics should be

$$\bar{V}_k = -\,Z\left(jk\omega_0 \right) I_k + U_k \qquad (9)$$

where $Z(j\omega)$ is the impedance of the linear network as seen at the diode terminals, and U_k is the Thévenin equivalent source voltage ($U_k \neq 0$ only for k = 0, m). Thus a set of nonlinear equations for the voltage harmonics is obtained by imposing

$$\bar{V}_k = V_k \qquad k = 0,\ 1,\ \ldots,\ N \qquad (10)$$

Once the solution of (10) has been obtained, all quantities of interest, including the circuit efficiency

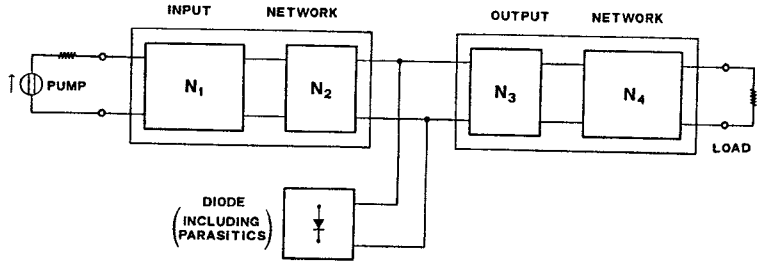

Fig. 2 Detailed topology of sample divider.

η, can be derived by a conventional analysis of the linear network.

From the *design* point of view, we first note that a conventional optimization of the linear network using the divider efficiency as the objective function is impossible. In fact, solving the system (10) to find η is usually a lengthy job, making the direct approach far too expensive in terms of computer time to be practically affordable.

The only alternative is to carry out a *simultaneous* search for both the voltage harmonics *and* the electrical parameters of the linear network. In order to do this we define an objective function of the form

$$F_{OB} = \left\{ \sum_{k=0}^{N} \left| \bar{V}_k - V_k \right|^2 \right\}^{\frac{1}{2}} + f(\eta)\ , \qquad (11)$$

where

$$f(\eta) = \begin{cases} \alpha\left(\eta - \eta_0 \right)^2 & \text{for } \eta \leq \eta_0 \\ 0 & \text{for } \eta \geq \eta_0 \end{cases} \qquad (12)$$

η_0 being the minimum required efficiency and α a suitable constant. According to the preceding discussion, F_{OB} is a function of the voltage harmonics V_k and of the linear network parameters, which can be minimized by conventional methods. This usually yields a complete design at much the same cost as one function evaluation of the conventional approach mentioned above, especially when the circuit variables are carefully selected. Failure to attain a minimum of the objective function close enough to zero indicates that the design specifications cannot be met; most likely this denotes an improper combination of pump available power, minimum efficiency and diode choice for the frequency range of operation. Notice that the diode bias voltage can be used as a design variable, providing a further degree of freedom and a better conditioning of the optimization problem.

A design example

As an example of application, we illustrate the design of a divider by 2 having a 20% bandwidth with an input center-band frequency f_{in} = 2.375 GHz and a maximum permitted loss of 5 dB at an input power level of 10 dBm. This divider acted as the first step of a dividing chain used to lock the tunable RF source of a 120 voice channel FM radio link to a 4 MHz reference oscillator.

As a first step, we choose the circuit topology schematically given in fig.2; the input network is designed as a band-pass filter with a 20% pass band around f_{in}, and the output network as a low-pass filter with cutoff frequency 1.1 (f_{in}/2). The input filter is realized by means of short circuited stubs $\lambda/4$ at f_{in}, while for the output filter a stepped-impedance topology is selected. The order of each filter is determined on the basis of a 15 dB minimum required isolation between the input and output ports across the input and output frequency bands. A silicon varactor † with a zero-bias depletion-layer capacitance C_{TO} = 3.3 pF and a quality factor of about 90 at f_{in} is selected, mainly for the sake of availability.

An analysis of this preliminary circuit configuration by means of (10) shows that frequency division does not occur in this circuit, since the only possible solution has V_1 = 0. As could be expected, selecting at random and assembling two filters and a diode does not mean building a frequency divider. Using this circuit as a starting point, an optimization of the linear network is then carried out in the way discussed in the preceding section with η_0 = 0.35. In order to save computer time, only the inner sections of the input and output filters are optimized (N_2, N_3 in fig. 2), while the rest is left unchanged at the initial configuration. Furthermore, only three frequencies (lower and upper bounds and center of the operating band) are considered in the optimization. In the resulting network frequency division is obtained with a maximum loss of 4.5 dB over the band of interest and a diode bias voltage of 0 V. The overall cost of the design in terms of computer time is about 180 sec on a CDC Cyber 76 computer system by use of a conjugate-gradient minimization algorithm and with N = 10 harmonics.

The final circuit layout is depicted in fig. 3. In this network the diode is self-biased, a DC return being provided by the short-circuited ends of the input filter stubs. A higher divider efficiency could be obtained by slightly forward-biasing the varactor; however, the zero bias voltage has the considerable advantage of completely eliminating any sort of bias network.

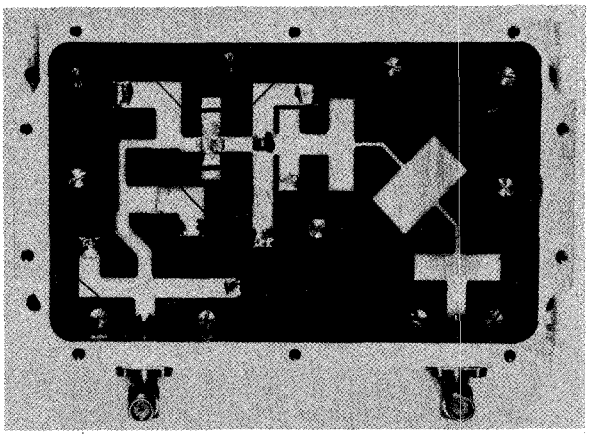

Fig. 3 Picture of MIC parametric frequency divider operating at 2.375 GHz

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